

EPE-PEMC Tutorial Sep. 2010

FPGA based High Performance Motor Control

Time schedule: 3h

Instructor:

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About the Instructor

Prof. Dr.-Ing. **Jens Onno Krah** studied electrical engineering at the University Wuppertal and obtained his PhD 1993 by Prof. Holtz within electrical drives research. Until February 2004 he worked as technical director for Kollmorgen, formerly Seidel Servo Drives. He was responsible for the development of the Kollmorgen Servo Drives. Since March 2004 Prof. Krah teaches control engineering at the University of Applied Sciences Cologne. Key research interests are high performance motor control and digital signal processing with programmable logic (FPGA).

Contents

High performance motion control is still a fast growing market segment. Especially the direct drive technology offers significant advantages in terms of reliability and machine size. More and more functions like feedback processing or field bus implementations are realized in Field Programmable Gate Arrays (FPGA). The advanced FPGA based control architectures are covered by discussing algorithms and new electronic components. Due to the innovation cycles of the semiconductor suppliers the size and the cost of the more and more complex servo drive systems is not increasing. Therefore the development, installation and set-up time (= cost) is a steady growing issue. Robust controller designs realized in programmable logic with clear set up procedures or reliable self-tuning algorithms can help to use these innovations utilizing a reasonable set-up time.

1. Motor Feedback Systems
 - Feedback options / resolution: encoder – resolver – sensor-less
 - FPGA based Resolver Digital Converter (RDC)
 - Digital feedback communication
2. Current Measurement - sampling versus $\Sigma\Delta$
 - $\Sigma\Delta$ Digital to Analog Converter (DAC)
 - $\Sigma\Delta$ Analog to Digital Converter (ADC)
 - Sinc decimation filter
 - Multi channel current processing
3. Current Control – System Models and Control Objectives
 - Usage of FPGAs for PWM generation and dead time generation
 - Predictor based digital control
 - FPGA based digital control (VHDL)
 - I²T estimation
 - Soft Core CPU Nios II
 - Parameter based tuning versus auto-tuning
4. Velocity Observer – System Identification and Model Order Reduction

- Speed measurement, acceleration measurement/estimation
 - Bandwidth – Low noise versus high speed
 - Auto-tuning
5. Velocity Control – Robust Controller Design
- Observer based digital control
 - Compliant load, filter, inertia ratio
 - Feed forward
 - Tuning guidelines
6. Position control
- Digital control feed forward generation
 - Second feedback
 - Trajectory generation
 - Tuning guidelines
7. Concluding Remarks